

REMARKS

Claims 1-51 are pending in the application. Claims 1-14, 20-26 and 28-45 are withdrawn from consideration. By this Amendment, Applicants add new claim 52.

Claim Rejections - 35 U.S.C. § 103

Claims 15-19, 27 and 46-51 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Sakamoto et al. (US Patent 6,281,446, hereinafter “Sakamoto”). Applicants respectfully traverse.

Preliminarily, regarding claims 46, 48, and 50, the Examiner asserts that Sakamoto anticipates the features of these claims “as best understood.” However, there is no objection to the claims or a rejection under 35 U.S.C. § 112 for indefiniteness. Applicants therefore respectfully request that the Examiner clarify any issues with the claim language.

The claimed invention comprises a method of manufacturing a circuit board in which substrates are laminated onto a motherboard. In contrast, Sakamoto discloses a circuit board formed by placing a carrier board 16 into a recess 15 of a motherboard 11 and securing the carrier board and motherboard together with connectors 23, which may be solder balls, gold bumps, or electrically conductive paste. See FIG. 1 and col. 4, lines 25-32.

Applicants submit that Sakamoto fails to teach “laminating” base materials as claimed. Sakamoto specifically discloses joining the carrier board 16 and the motherboard 11 with connectors 23. In spite of the Examiner’s assertion to the contrary, Applicants submit that heating and pressing the two boards would not have been obvious to a person of ordinary skill in the art. In order to join two components via connectors made of solder balls, gold bumps, or electrically conductive paste, only the connectors must be heated. Applicants submit that it would not have been obvious to a person having ordinary skill in the art to have heated the entire

board being mounted. Such a step would not be necessary to join the materials by solder, gold bumps, or electrically conductive paste.

Furthermore, Applicants submit that Sakamoto teaches away from lamination. As seen in col. 2, lines 21-27 of Sakamoto, laminating boards together may possibly have been known in the prior art, but “there are problems from delaying the electrical signal due to the increase of the length of the wiring lines, the increase of total thickness of the wiring boards, and that the flatness is insufficient or the height is not low enough.”

Therefore, Applicants submit that Sakamoto does not teach or even fairly suggest every feature of independent claims 15, 16, and 27, and in fact teaches away from these features. Applicants submit that these claims are therefore patentable over the cited art. Applicants further submit that claims 17-19 and 46-51 are patentable over the cited art at least by virtue of their respective dependencies.

New Claim

By this Amendment, Applicants add new claim 52. Applicants submit that the features of claim 52 have support in the present specification at least at FIGS. 4, 16, 21, 23, and 28.

Applicants submit that new claim 52 is patentable at least by virtue of its dependency from independent claims 15, 16, and 27. Furthermore, Applicants submit that a base material having a wiring circuit of Sakamoto is layered on the entire region in a front surface of a motherboard, i.e. the bottom surface of a cavity 15, and not a partial region as claimed.

Applicants therefore submit that Sakamoto does not disclose, teach, or fairly suggest the features of new claim 52.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

/ Carl J. Pellegrini cjp / 40,766
Howard L. Bernstein
Registration No. 25,665

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

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